HW Counter Discussion Summary

- **Topic: HW Counters support on Intel and AMD processors**
  - HW counter support for precise monitoring
    - IBS - instruction-based sampling (AMD)
    - PEBS - precise event-based sampling (Intel)
  - everyone now understands how PEBS in combination with LastBranch record information is used to recover IP

- **Topic: OS support**
  - everyone has an understanding of problems with the approach being pursued to integrate PEBS & IBS support with perf_events
    - no IBS support without kernel patch until 2.6.36 (Cray, take note!)
    - perf_events support using PEBS and LBR is unintuitive for calls
    - Intel ref and core cycle counts alias with perf_events interface
    - capturing off-core response events is problematic with perf_events requires two MSR; perf_events can’t schedule this
  - understand how one can monitor and attribute time to blocking system calls using perf_events monitoring + TSC register
  - we understand the issue getting detailed IBS and PEBS info from perf_events. we wish stephane luck convincing them!
HW Counter Discussion Summary (2)

• **Topic: Driver issues**
  — Intel has a driver for accessing HW counters on Intel processors
    – provides system wide view
  — HPCToolkit wants’s interrupts delivered to threads for call stack unwinding
  — sketch of an approach to adapt the driver for Rice needs

• **Topic: PAPI support**
  — PAPI support for Intel processors developed using manual “3B”
  — some counters are known to be problematic
  — David Levinthal described how to obtain verified information about useful counters

• **Topic: Diagnosing performance bottlenecks on Intel chips**
  — David Levinthal will supply sets of useful events for diagnosis
  — David Levinthal has diagnosis tree that he will disseminate

• **Topics: DOE license for Intel tools; common file format**