Performance Analysis on Petaflop clusters

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Petaflop scale analysis methodology

- Most slides taken from

  - 60 slide presentation on Xeon 5500 microarchitecture
    - Introduction

  - 190+ slide presentation on HW event performance analysis/sw optimization
    - What would I do with 100 million lines of code when told to just make it go fast
Basic performance analysis and SW optimization methodology

- Tune the machine
  - Make sure bios, dimms, disks etc are correctly configured

- Tune the compiler usage
  - only optimize what uses time

- Remove the pipeline stalls

- Remove the single thread resource limitations

- **Improve the scaling**
A Hypothetical Petaflop Cluster

• Not based on any existing or future planned processor known to the author
• Assumptions
  – 24 DP Gigaflops per core
    – 3 Ghz/core – and AVX instruction set
  – 1.2 Teraflops/box
    – 50 cores
  – 850 boxes

Note: many of these slides taken from:
Scaling on large clusters of multicores

• Large cluster MPI job scaling tends to be limited by all-to-all MPI APIs
  – \( N \times \log(N) \) or even \( N! \) (if really badly coded 😊)

• Experience has shown that using shared memory threading within the box can be used to reduce the MPI node count substantially.

• The result of such a combination is that the node count is not largely higher than today's clusters, but multi thread scaling must be improved.
Event Classes: High Level View

1. Execution flow events
   - Cycles, Branches, stalls, uops/inst_retired
   - Guide compiler usage

2. Penalty events (ONLY useful if they have well defined cost)
   - Ex: load requiring access to dram
   - Modify code/build to reduce penalties/pipeline stalls

3. Resource saturation events
   - Bandwidth, load/store buffers, dispatch ports
   - No well defined cost
   - Change data layout/access patterns

4. Architectural characterization
   - Cache accesses, MESI states, snoops
   - Used to improve silicon design, not application performance

5. Instruction mix
   - Do not measure what you think, extremely difficult to validate
Less than ideal multi core scaling

• Perfect scaling results in the number of perf events (summed over cores) being constant

• Difference of event counts can identify locality using cycles and some reasons for non scaling behavior
  – Cacheline access contention can cause non scaling
    – Load-hitm and store address analysis identifies this

• Most non scaling due to resource saturation and evaluated as a ratio: events/wall_cycles
  – Wall_cycles ~ cycles/active cores
    or Cpu_clk_unhalted.thread max(ICPU)

  – Cannot be seen in difference display
Superfluous sources/signatures of non scaling

• Turbo
  – Having this on results in large drop from 1->2

• Smaller share of LLC
  – Decrease in LLC hits, increase in LLC miss

• Increase in page faults
  – More threads require more memory

• Asymmetry associated with core 0
  – OS induced imbalance

• Context switching
  – OS’s love to move things around, being the boss!
  – Don’t know about logical cores & double up on one physical core, while other phys cores are idle
Sources/signatures of non scaling

• Saturating a resource
  – Ex: Bandwidth
  – Code optimization increases resource saturation

• Shared memory application specific
  – Serial execution
  – Overly contested lock access
  – False sharing (non overlapping access to a line)

• NUMA based non scaling
  – Increase in *.remote_dram
Expanding the “arrow” we see the 2 threads access the line at Different Offsets...This is False Sharing.
More sources of non scaling

• Load imbalance
  – Increase in halted cycles

• MPI global operations
  – increase in time associates with MPI global APIs
    – Ex: allreduce

• Synchronous message passing
  – “Intrinsically” non scaling

• HT can be viewed as a way to recover scaling
Dominant issues

• Within the box
  – Thread interactions (hitm/store analysis)
  – Serial portion
  – Threading decomposition load imbalance

• Over the cluster
  – MPI all to all
  – Load imbalance
Resolving non scaling issues

- Disable turbo while doing measurements
- Disable HT while doing measurements
- Pin all affinities
  - OS’s love to move things
  - Old OS’s will schedule 2 threads on a physical core while leaving other physical cores idle. This increases with thread count
- Make sure there is enough memory
  - /proc/meminfo->Active (?)
- Do 1 thread baseline on a core other than 0
- Increased LLC miss
  - Usual approaches to fixing these, see large talk
Resolving non scaling issues

• Bandwidth issues
  – Check data decomposition for separation
  – Improve data layout to reduce cacheline consumption
  – See previous section on BW issues

• Excessive lock contention
  – Use finer grained locking
  – Use faster locking APIs
  – Make sure the global update is really needed
    – Can you continue working with local copy

• False sharing
  – Put 64 bytes between data elements
Resolving non scaling issues

• NUMA related non scaling
  – Remote dram data access
    – Improve buffer initialization for local access
    – Make multiple copies for each socket
  – Remote dram ifetch access
    – Make two binaries on the disk and affinity pin per socket

• MPI global operations
  – Use OpenMP (Cilk, TBB, Pthreads) within a box to reduce MPI nodes
  – Use good MPI library
Resolving non scaling issues

• Load imbalance
  – Seen as halted cycles
    – TSC difference for successive cpu_clk_unhalted.ref != SAV
  – Work queue approach dynamically restores balance
    – At a cost
      – NUMA locality can be lost
      – SW prefetching can become unpredictable within a thread
  – Estimate work during data decomposition to create balanced work rather than balanced iteration count
  – Save some iterations for final work queue balancing
Summary

• Petaflop scaling problem can be reduced to single box thread scaling for many issues
• Event based sampling performance analysis is extremely powerful
• Correct methodology is essential
• Correct usage of events is essential