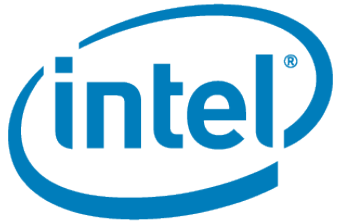

Performance Monitoring on Intel® Core™ i7 Processors*

Ramesh Peri
Principal Engineer & Engineering Manager
Profiling Collectors Group (PAT/DPD/SSG)
Intel® Corporation
Austin, TX 78746

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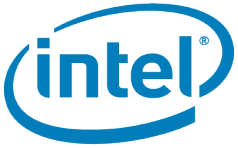

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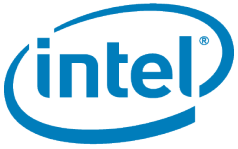
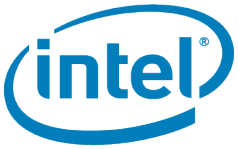


Agenda

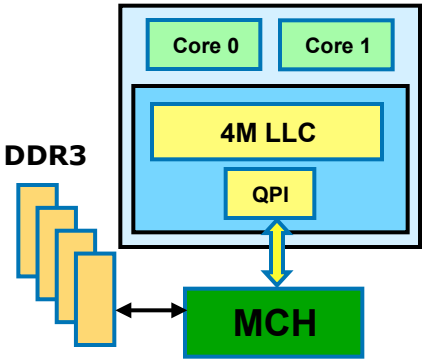
Goal: Provide a sample of the PMU features of Core™ i7

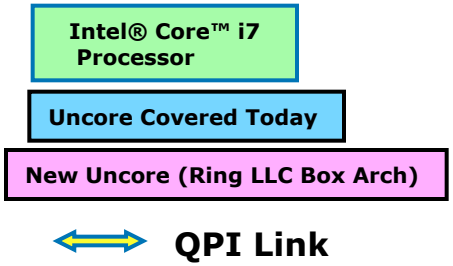
- **Core™ i7 Processor Architecture Overview**
- **Performance features of Core™ i7**
  - **Loop Stream Detector**
  - **Macro-Fusion**
  - **Memory Access**
  - **False Sharing**
  - **Load Latency Threshold**



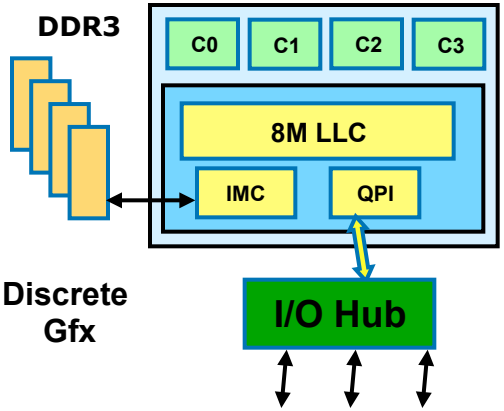
Platforms

Mobile/Desktop

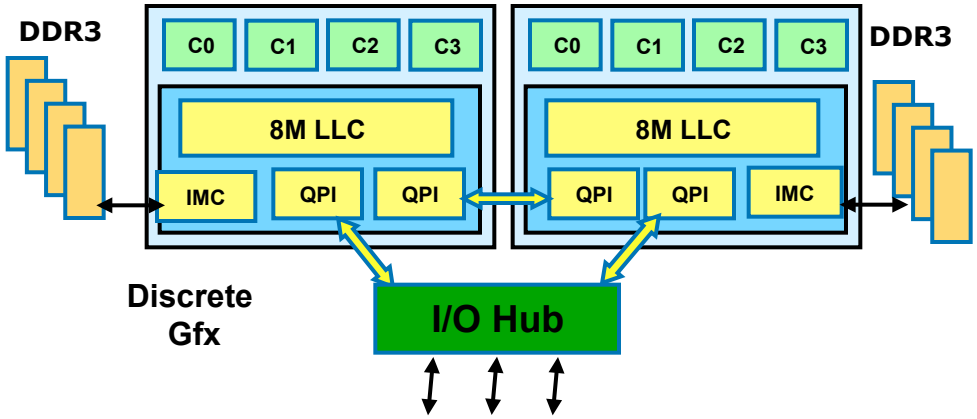




HE Desktop /mobile UP server & WS



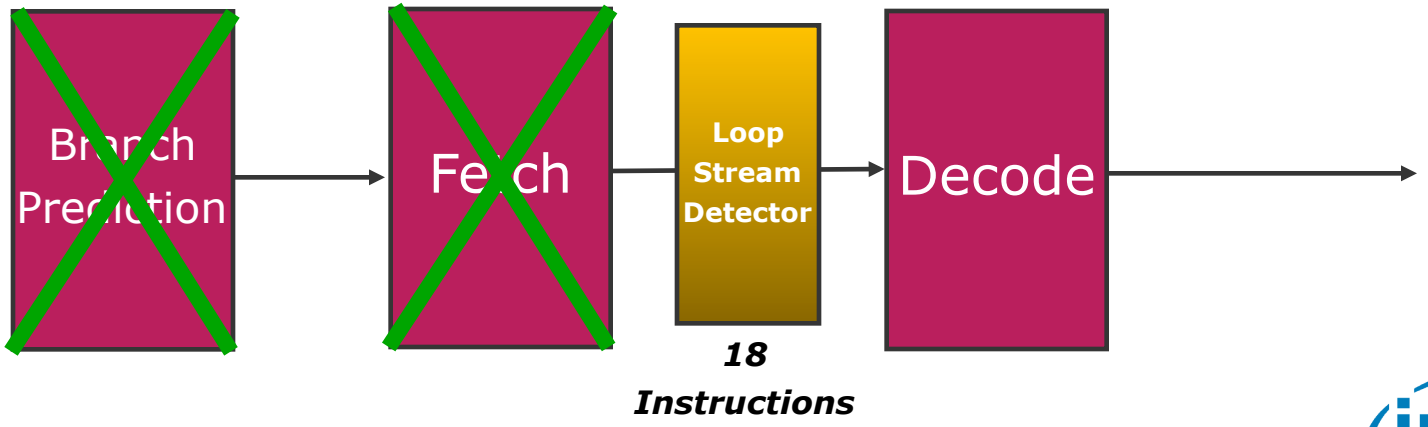
DP Servers & WS

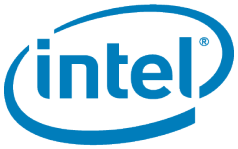


Loop Stream Detector - Recap

- Loops are very common in most software
- Take advantage of knowledge of loops in HW
  - *Decoding the same instructions over and over*
  - *Making the same branch predictions over and over*
- Loop Stream Detector identifies software loops
  - Stream from Loop Stream Detector instead of normal path
  - Disable unneeded blocks of logic for ***power savings***
  - ***Higher performance*** by removing instruction fetch limitations

Core 2 Loop Stream Detector

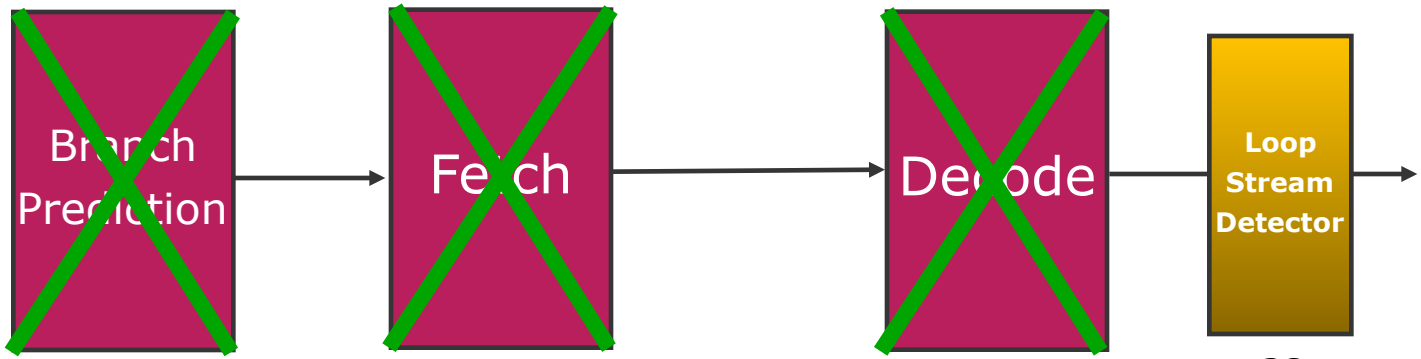




Core ™ i7 Loop Stream Detector

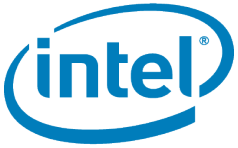
- Same concept as in prior implementations
- ***Higher performance:*** Expand the size of the loops detected
- ***Improved power efficiency:*** Disable even more logic

Nehalem Loop Stream Detector

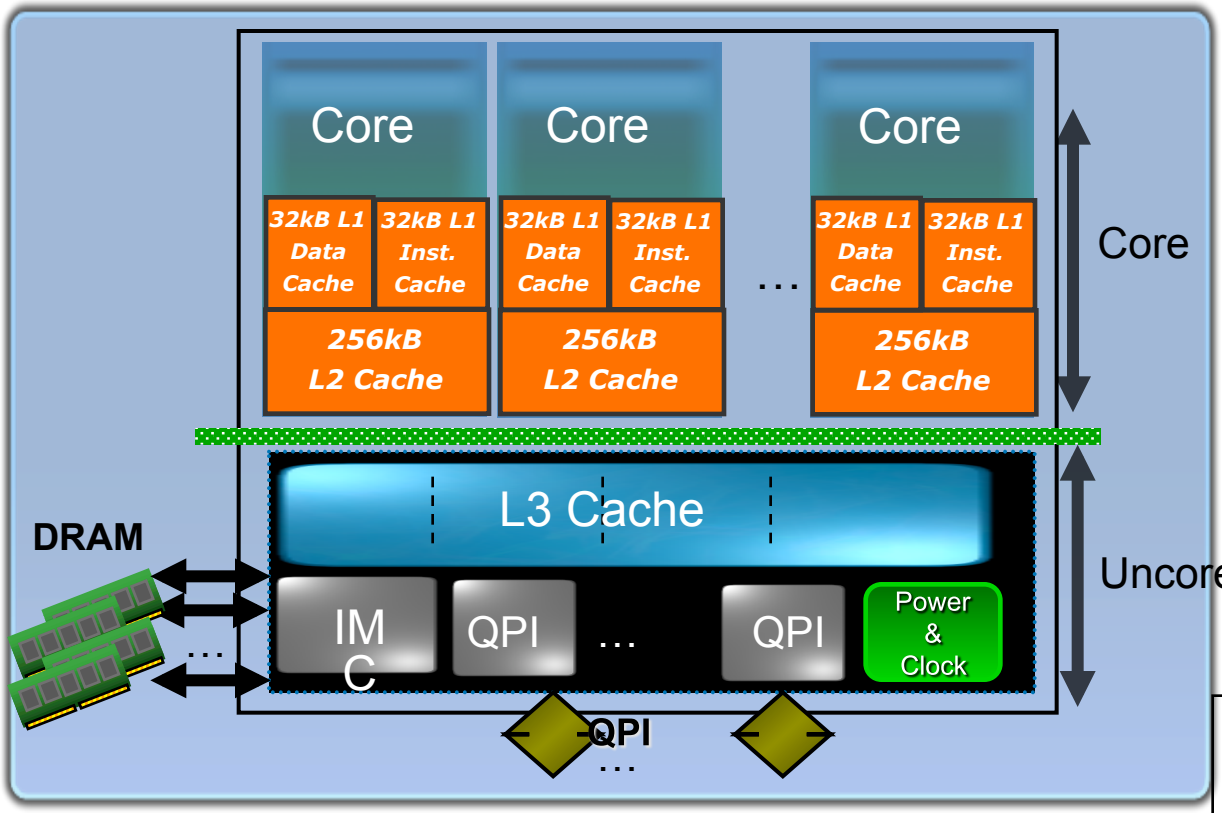


Loop Stream Detector – is it working ?

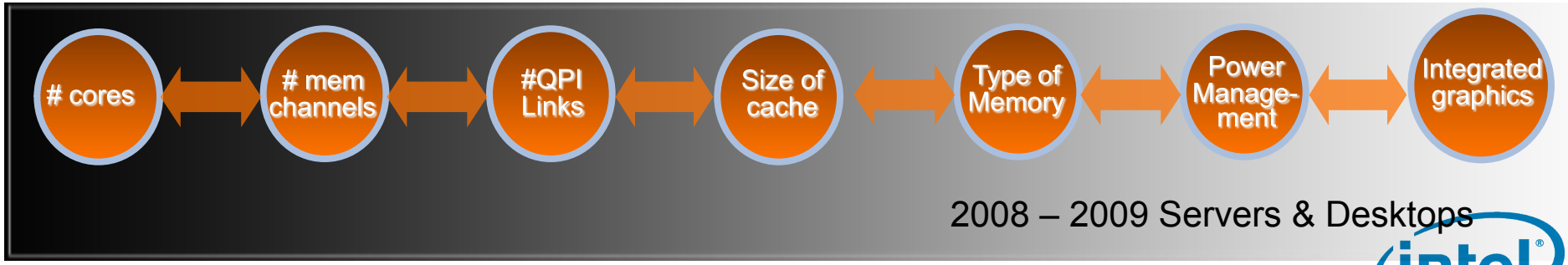
- LSD.UOPS is an event which provides the number of uops delivered by loop stream detector
- A tool which can tell
  - For every hot loop in the program whether the loop stream detector is active for that loop or not



Core™ i7



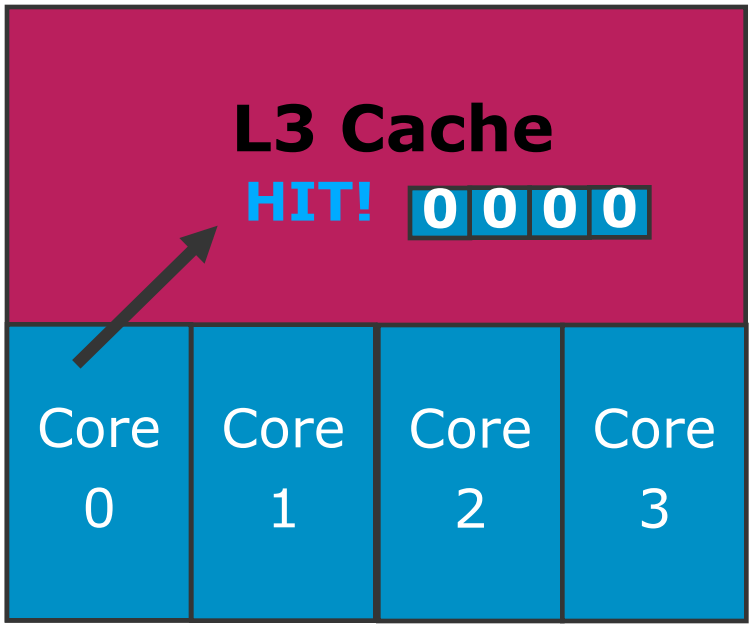
Differentiation in the "Uncore":



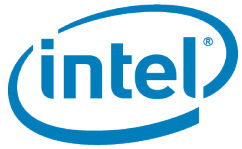
L3 Cache

- **L3 is inclusive with respect to L1 & L2**
  - **Provides good scalability**
  - Is implemented by maintaining a set of "core valid" bits per cache line in the L3 cache

Inclusive



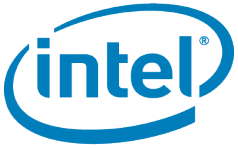
Core valid bits limit unnecessary snoops



Some PMU events using this feature

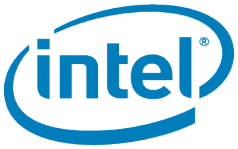
- MEM_UNCORE_RETIRED.OTHER_CORE_L2_HITM
  - Load instructions retired that HIT "modified" data in sibling core
- MEM_LOAD_RETIRED.OTHER_CORE_L2_HIT_HITM
  - Load instructions retired that HIT "modified" or "unmodified" data in sibling core

These events can enable many capabilities like true/false sharing, race detection tools



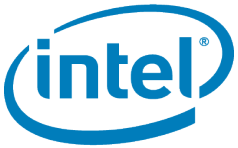
Some limitations of these events

- No Store HITM
  - Currently only Load HITM
- No ability to identify the source core id of the access
- No ability to raise PMI based on address range for data addresses
- PEBS EIP puts current EIP
  - which is the next instruction address
  - Requires some clever techniques and effort to figure out actual address
- HITM in the presence of SMT is not useful



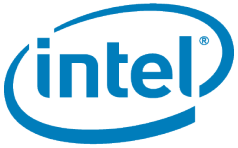
Macro Fusion - Recap

- Introduced in Core™ 2 Microarchitecture
- TEST/CMP instruction followed by a conditional branch treated as a single instruction
  - Decode as one instruction
  - Execute as one instruction
  - Retire as one instruction
- Higher ***performance***
  - Improves throughput
  - Reduces execution latency
- Improved ***power efficiency***
  - Less processing required to accomplish the same work



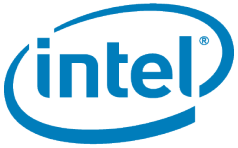
Core™ i7 Macro Fusion

- Goal: Identify more macrofusion opportunities for increased ***performance*** and ***power efficiency***
- Support all the cases in Core™ 2 Microarchitecture **PLUS**
  - CMP+Jcc macrofusion added for the following branch conditions
    - JL/JNGE
    - JGE/JNL
    - JLE/JNG
    - JG/JNLE
- Core™ only supports macrofusion in 32-bit mode
  - Core™ i7 supports macrofusion in both 32-bit and 64-bit modes



How effective is Macro Fusion ?

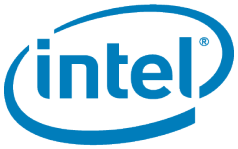
- MACHINE_CLEARS.ASSIST_FUSION
  - Counts the number of fusion assists
- Ensure that “all” appropriate CMP/Jxx sequences are all fused



False Sharing
What is it and why is it a Problem

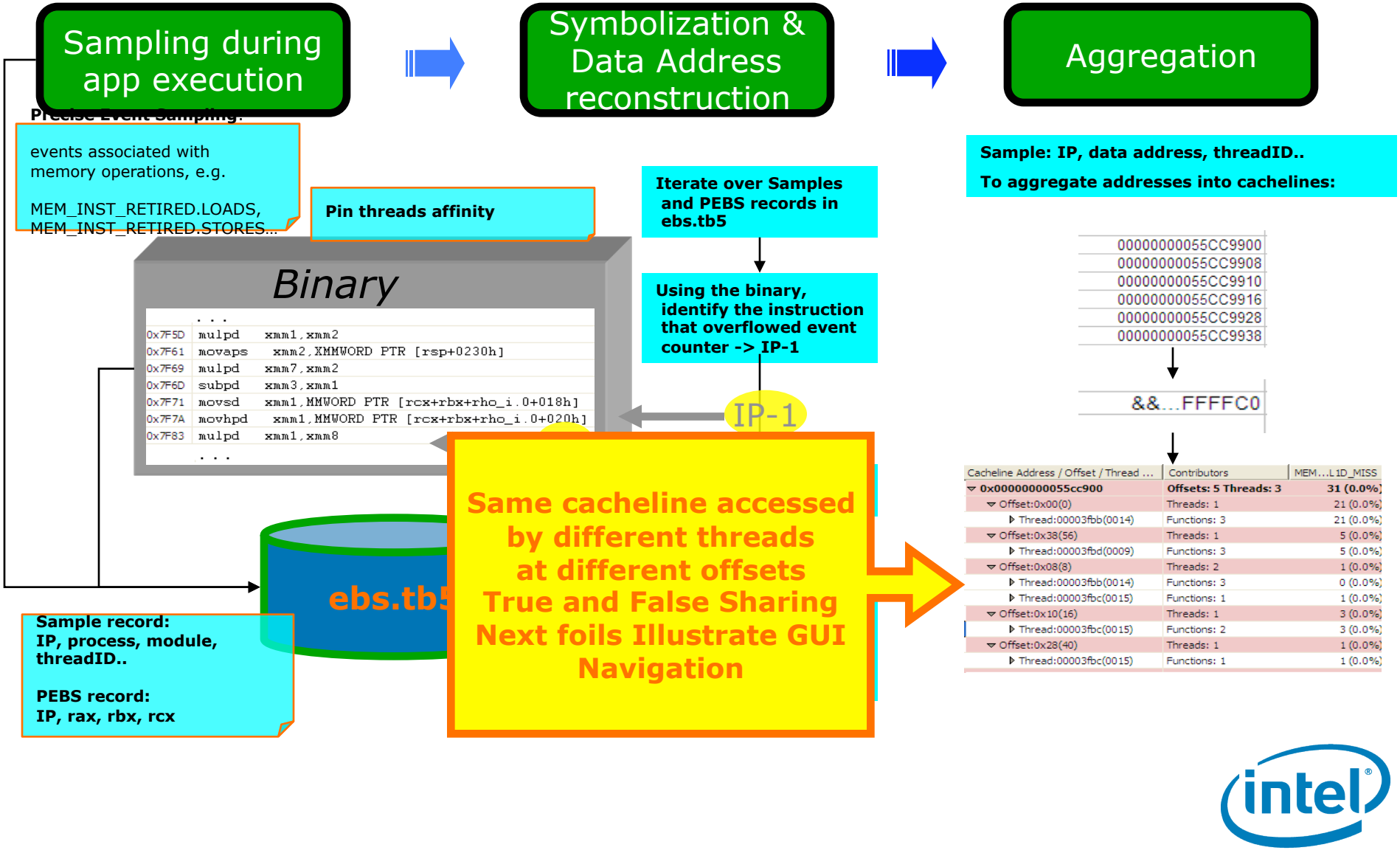
- Cache coherency protocols require that all cores use the most current version of every cacheline
- Shared lines can be modified by any thread
  - Causing lines to be renewed regularly, if any thread writes to any byte in the line
    - (replace an invalid state copy with new valid copy)
  - Line renewal can cause a cache miss by other threads
  - and a 40-300 cycle execution stall
    - Depending on cacheline location
- False sharing is when different threads access non-overlapping regions of a cacheline

False Sharing Causes Avoidable 40-300 Cycle Stalls For Every Read Following a Write by Another Thread

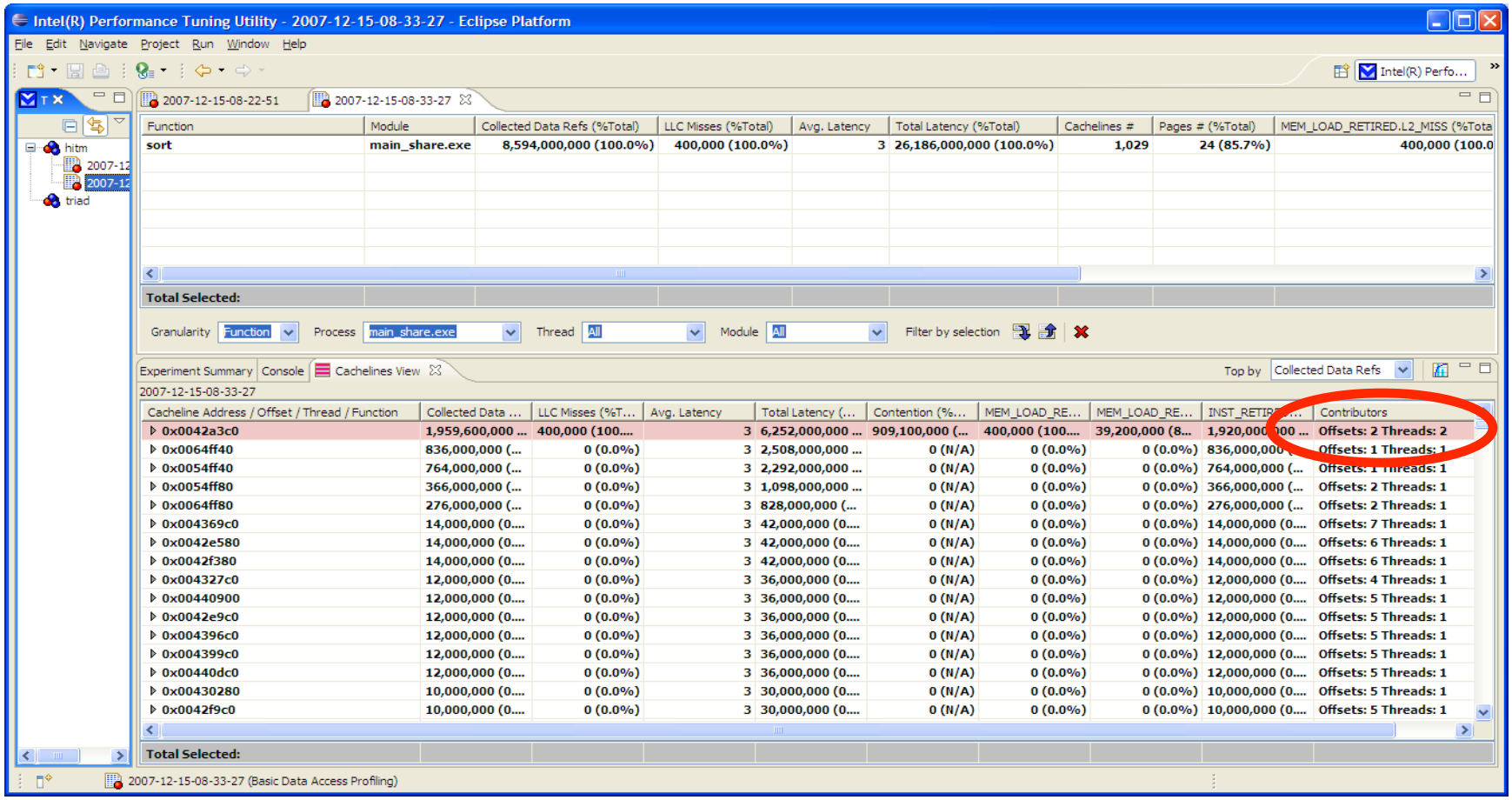


This foil is best viewed in animation mode

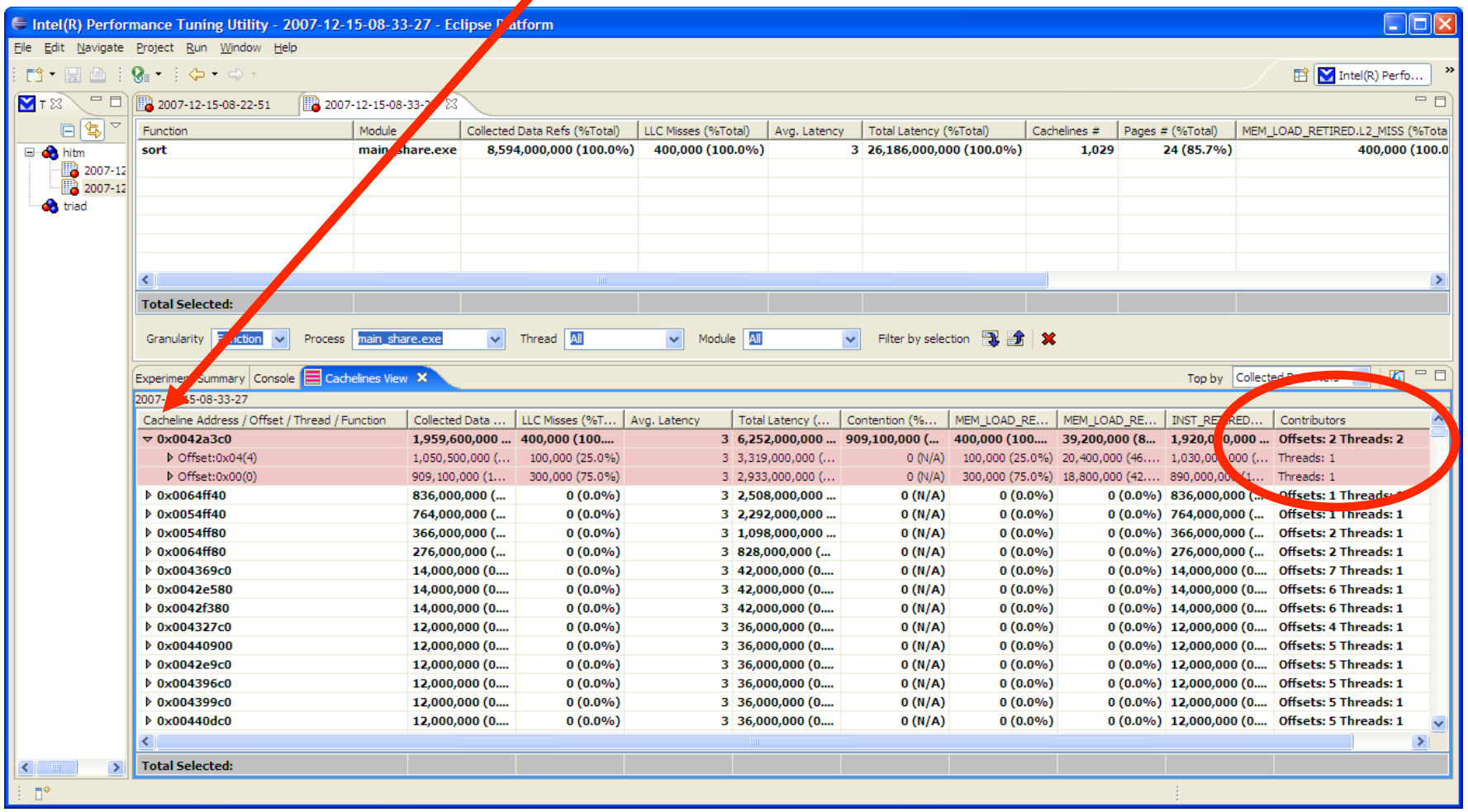
Data Address Profiling and False Sharing Detection



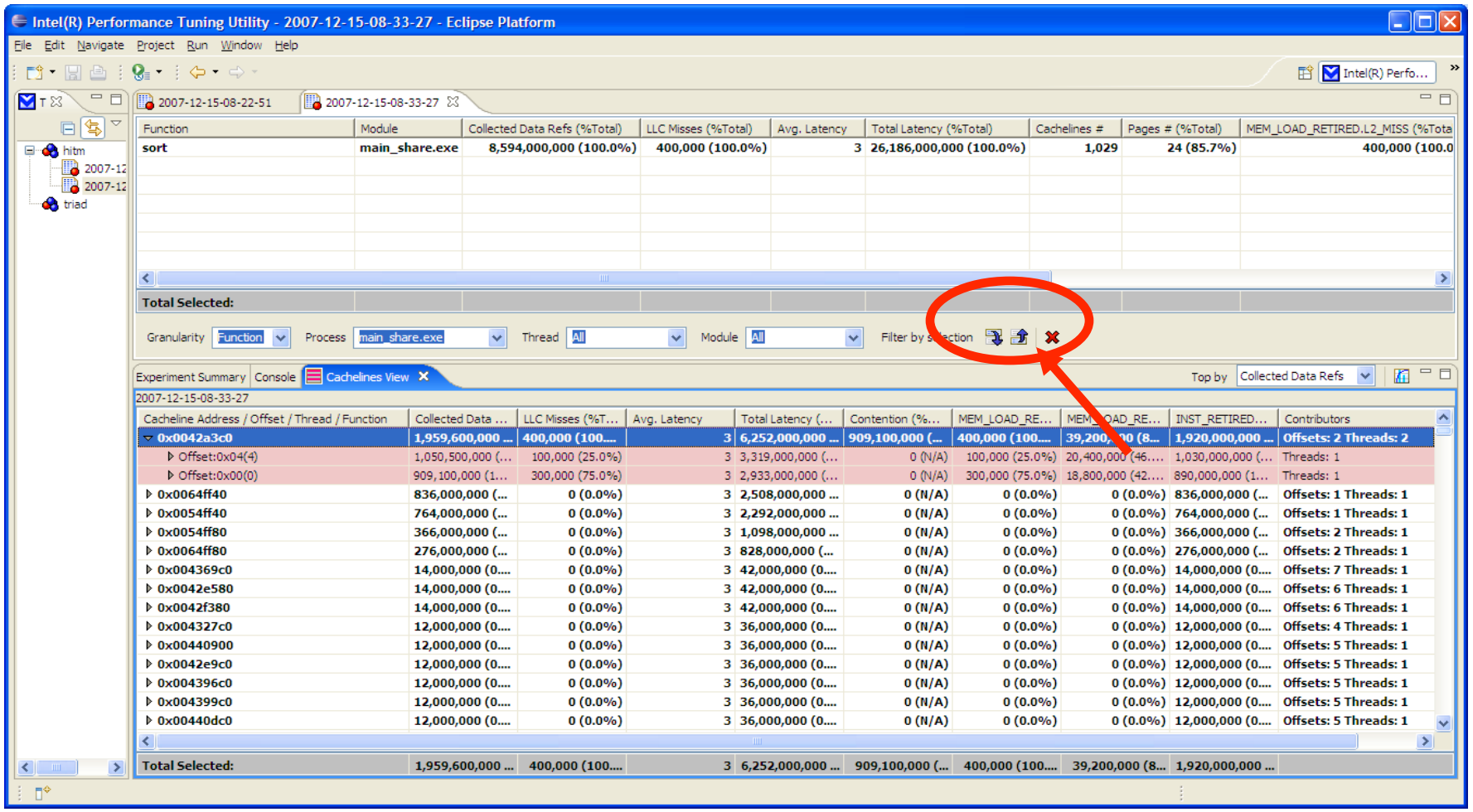
Synthetic Example: Heavy Contention on this Line -- Multiple Threads Accessing Different Offsets Indicate False Sharing (Identified by Rose Highlighting)



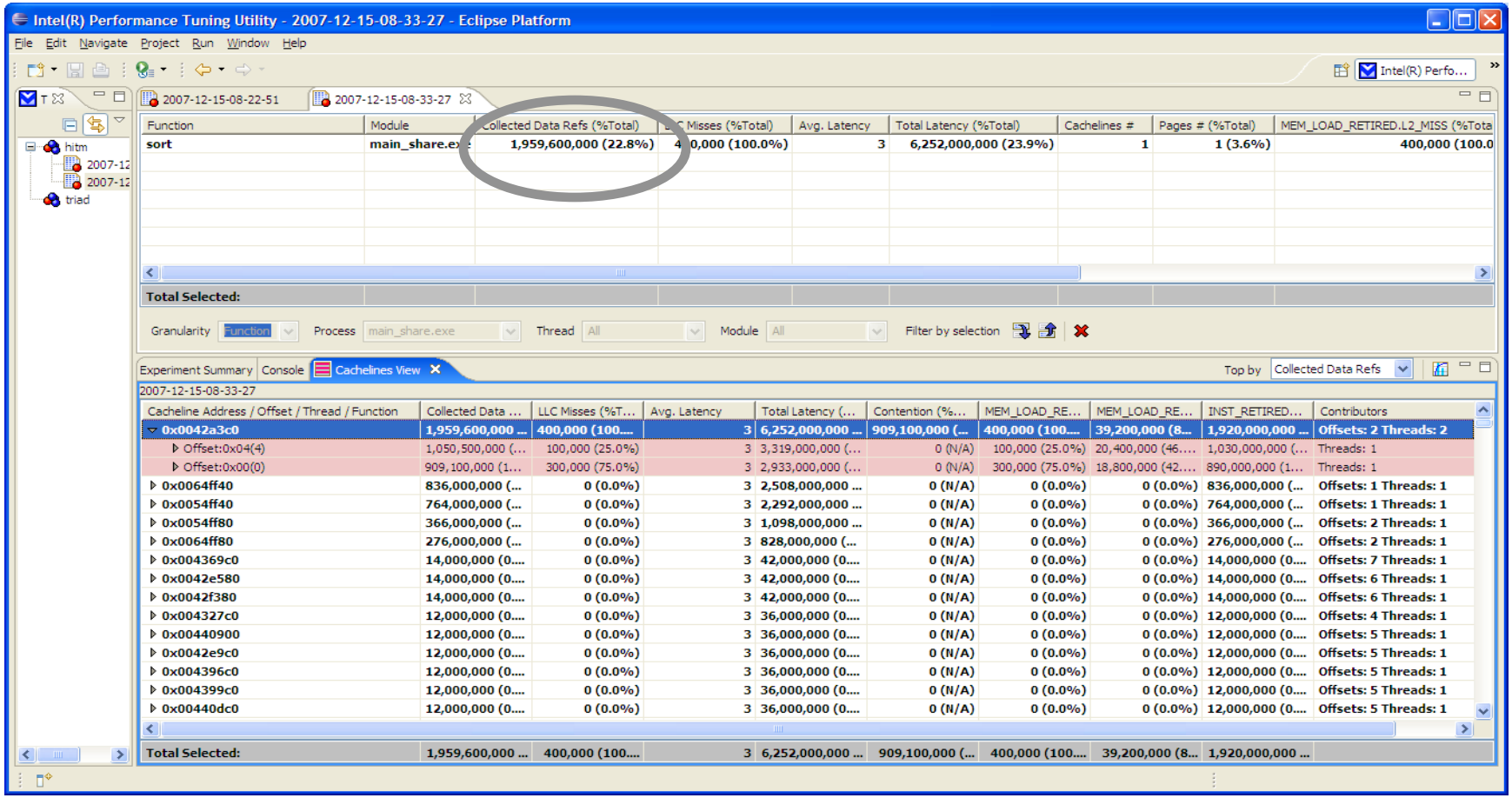
Expanding the "arrow" we see the 2 threads access the line at Different Offsets…This is False Sharing



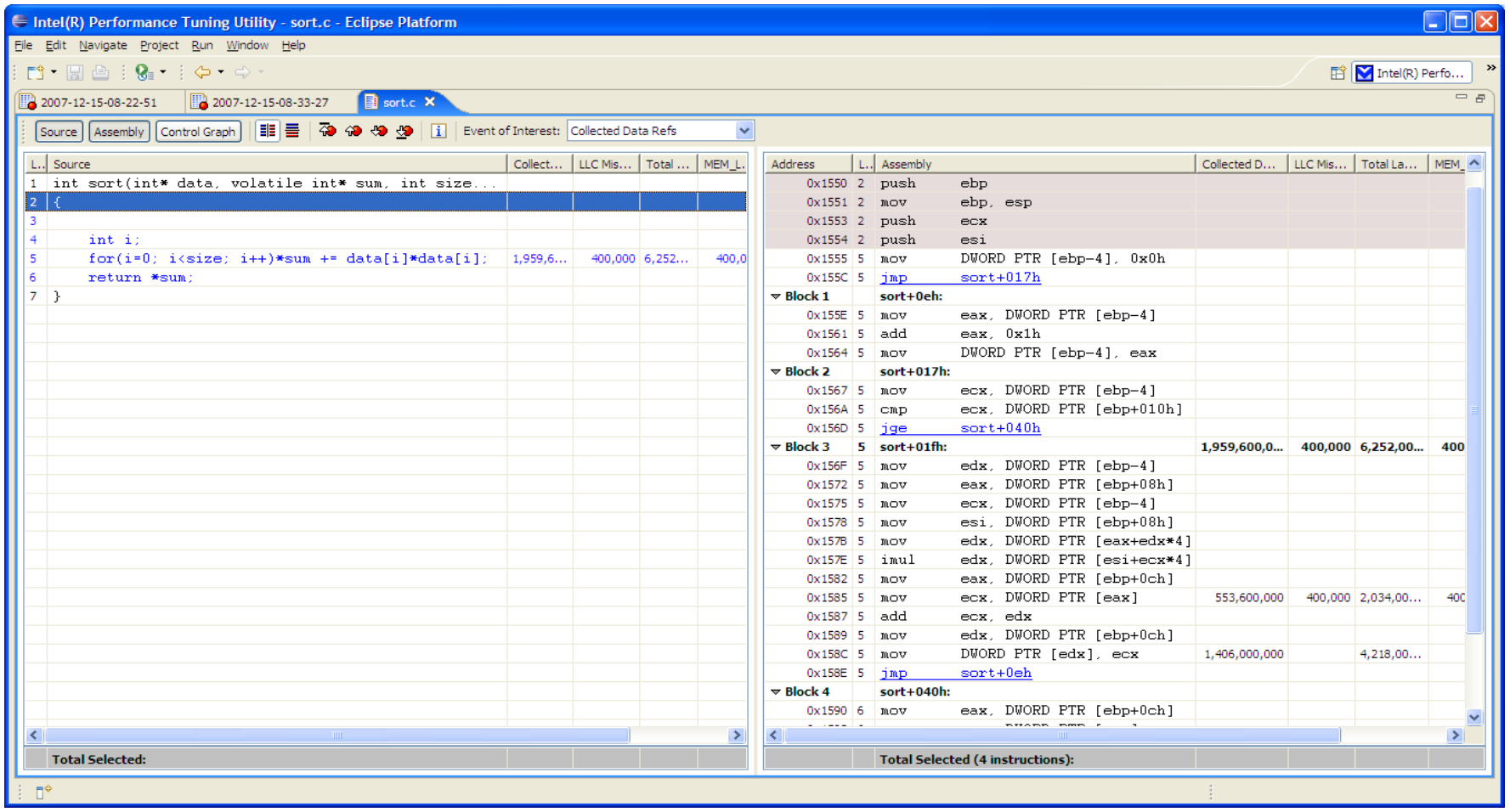
Select the falsely shared cacheline (now blue) and Filter the Hotspot view to only Display Accesses to that Line (multiple lines also work)



Only Events Referencing the Selected Line(s) are now in the Hotspot View Double Click to reach source/ASM view



The Pointer "sum" is Causing the False Sharing

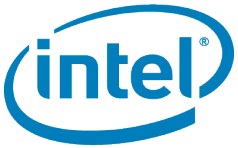


Load Latency Threshold Event

- **Ability to trigger count on minimum latency**
  - **Core cycles from load execute->data availability**
- **Linear address in PEBS buffer**
  - **Allows driver to collect physical address**
  - **Only total measurement of local/remote home access**
- **Data source captured in bit pattern**
  - **Actual NUMA source revealed**
- **Only ONE latency event/min thresh can be taken per run**
  - **Minimum latency programmed with MSR**
  - **Global per core**
    - **0x3F6 MS_PEBS_LD_LAT_THRESHOLD bits 15:0**
- **Can use to detect a variety of properties about memory accesses**
  - **Local vs remote etc.**
  - **Can be filtered at with hot spots to detect causes for them**

Call to Action

- **Download PTU from http://software.intel.com/en-us/articles/intel-performance-tuning-utility/ and have fun**
  - **Makes all the events of Core™ i7 available**
- **If you have any questions or comments you can reach me at ramesh.v.peri@intel.com or ask them in the discussion forums at http://software.intel.com/en-us/forums/**



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